CLAIMS

What is claimed is:

1. A method of forming an interconnect in an oxide isolation region immediately adjacent to an active area of an integrated circuit, comprising:

masking the active area with a nitride layer, wherein an edge of the nitride layer is aligned with a lateral edge of the active area that abuts the oxide isolation region;

exposing the oxide isolation region and a portion of the nitride layer to an etch process that etches the oxide isolation region faster than the nitride layer such that a portion of the oxide isolation region is removed to form a downwardly extending opening in the oxide isolation region that exposes a portion of the lateral edge of the active area; and

at least partially filling the opening with a polysilicon material such that the polysilicon material contacts the active area to form the interconnect.

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2. A method of forming an interconnect in a dielectric isolation region immediately adjacent to an active silicon area of an integrated circuit, wherein the dielectric isolation region and the active silicon area share a common vertical interface, the method comprising:

masking a region of a top surface of the active silicon area with a nitride layer, wherein a lateral edge of the nitride layer is aligned with a lateral edge of the active silicon area along the common vertical interface;

exposing a selected area of the dielectric isolation region and a portion of the nitride layer to an etch environment that etches the dielectric isolation region faster than the nitride layer such that a portion of the dielectric isolation region is removed to form a downwardly extending opening in the dielectric isolation region that exposes a portion of the active area vertical interface; and

filling the opening with a polysilicon material such that the polysilicon material contacts the active area to form the interconnect.

3. The method of claim 2, wherein the dielectric isolation region comprises borophosphosilicate glass.

4. The method of claim 2, wherein the nitride layer is vertically separated from the active area by a layer of oxide.

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5. A method of forming a structure on a substrate assembly, the method comprising:

providing a vertical edge of an active area within an integrated circuit substrate assembly;

forming a region of dielectric material immediately adjacent to and in contact with the vertical edge of the active area;

forming a nitride layer above the active area and in alignment with the vertical edge;

etching a hole into the region of dielectric material at the vertical edge, wherein the hole is etched with an etching process that selectively etches the region of dielectric material at a faster rate than the etching process etches the nitride layer such that the active area is not etched; and

filling at least a portion of the hole with a volume of electrically conductive material within the region of dielectric material, the volume of electrically conductive material being situated in contact with the vertical edge, the region of dielectric material making a planar interface in contact with the vertical edge.

6. The method of claim 5, wherein forming the region of dielectric material comprises:

etching a trench through a sacrificial covering layer; and

filling the trench with a dielectric material.

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7. A method of forming an interconnect structure on an integrated circuit, comprising:

forming a silicon nitride layer above a silicon substrate of the integrated circuit;

etching a trench through the silicon nitride layer and into the silicon substrate to expose a vertical edge within the silicon substrate that is orthogonal to a top plane of the substrate;

filling the trench with a dielectric material to form an isolation region;

etching a hole into the isolation region at the vertical edge with an anisotropic etch to selectively etch the dielectric material at a faster rate than the anisotropic etch etches the silicon nitride layer;

forming a polysilicon plug within at least a portion of the hole such that the polysilicon plug is situated to the side of, in contact with, and immediately adjacent to the vertical edge and such that the polysilicon plug forms a planar and vertical interface with the silicon substrate; and

implanting dopants into the silicon substrate to form an active region adjacent the vertical interface.

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